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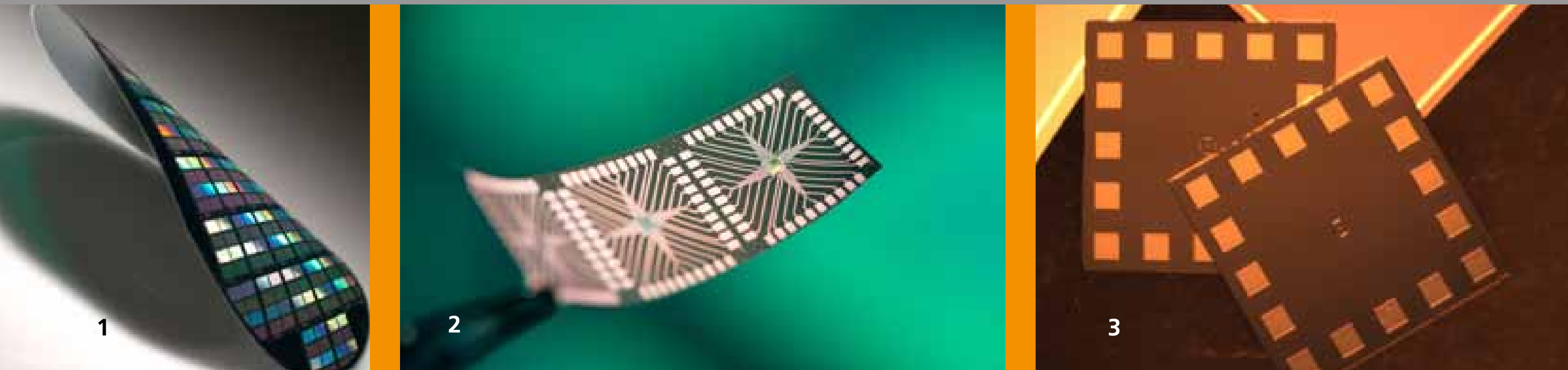

1 *Ultra-thin silicon device wafer*
2 *25 µm microcontroller chip in flexible foil package*
3 *Technology example for plasma dicing*

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FROM ULTRA-THIN SILICON DIES TO FLEXIBLE CHIP FOIL PACKAGES

Applications

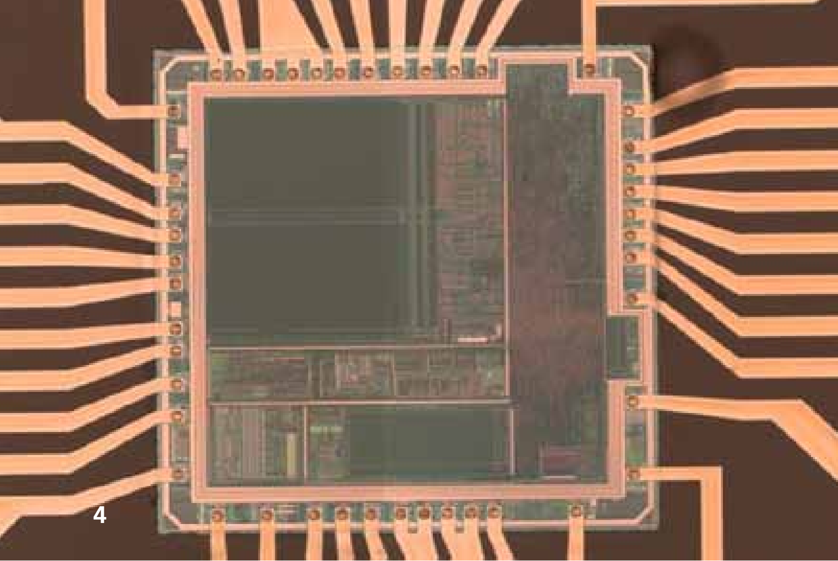
Lower height for chip packages is crucial for electronic components in mobile and wearable applications. Furthermore, the capability to bend and mount chip packages onto curved surfaces or into application specific formed housings will allow for the distribution of electronic and sensing systems in industrial production environments as well as in potentially any object of our daily life, e.g.

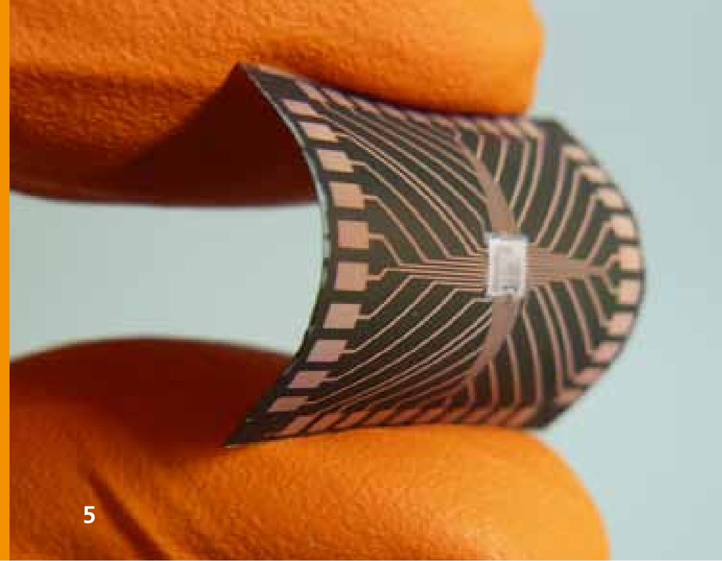
- Healthcare
- Wearable electronics
- Sensors on curved surfaces
- Robotics
- Smart packaging
- Internet of things-applications

Technical Innovation

Fraunhofer EMFT follows a so-called hybrid integration approach: We combine ultra-thin and flexible silicon ICs with film based circuitries and further thin electronic components. For the realization of the complete flex integration process Fraunhofer EMFT uses and offers its long-term experience and technological equipment for:

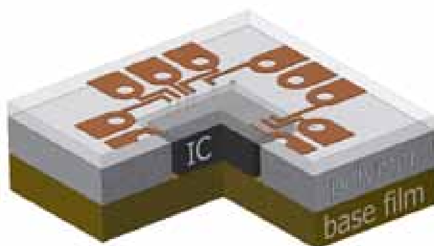
- Advanced wafer thinning (grinding, wet or dry etching, CMP polishing)
- Thin wafer handling, temporary bonding, specific focus on mobile electrostatic carriers (e-carrier)
- Die separation: here we propose the patented "dicing-by-thinning" concept, specific target is plasma dicing of ultra-thin wafers using e-carrier substrates for wafer handling





- Ultra-fine line patterning of metal wiring on flexible films (PET, PEN, PI) by roll-to-roll processing allowing line / space geometries of 20 µm
- High accuracy die bonding by automated equipment or self-alignment techniques
- Roll-to-roll and sheet-to-sheet processes for printing, lithography, metallization, etching, laser treatment, electroplating, lamination, coating, electrical testing and others

According to our patented "Thin Chip Foil Package" the ultra-thin dies are placed and embedded in a cavity of a multi-layer film laminate. Thereby the fragile IC is securely embedded in the center layer of a plane-parallel film package. The foil package represents a fan-out interposer for the I/O contact pads of the IC device (see figure below).



State of Development

The "Dicing-by-Thinning" concept was used to prepare 25 µm thin microcontroller devices, front side chip grooves were performed by standard sawing process, wafer thinning was done by grinding (DISCO DFG 8540) and chemical mechanical polishing (CMP, Avanti).

For preparation of the first „Thin Chip Foil Package" demonstrators we used polyimide films, which were temporarily attached onto silicon carrier wafers. This configuration allows to process thin film interconnects and the redistribution layer by standard lithographic patterning processes and equipment. It also allows for preparing a large number of film packages in parallel. Thin ICs were placed on the base film at high alignment accuracy (die bonder Panasonic FCB3). Figures 2 and 5 show the technological result of a set of chip foil packages after separation and removal from the carrier and figure 4 shows a microscopic view on the surface of the finally embedded and electrically interconnected ultra-thin microcontroller device.

Outlook

The technological concept allows for subsequent adaptation to a continuous roll-to-roll process for chip embedding in film substrates. This would enable extremely thin and flexible packages for any type of functional IC devices in high volume and at low cost. Fraunhofer EMFT intends to foster cooperative works with industrial partners for equipment development and product applications. We consider our concept for a "Thin Chip Foil Package" as a key enabling technology for many future products which require extremely flat form factor or mechanical flexibility.

Funding

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4 *Microscopic view on the surface of the finally embedded and electrically interconnected ultra-thin microcontroller device*

5 *Fan-out Demonstrator of a flexible "Chip Foil Package"*