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EMFT

FRAUNHOFER RESEARCH INSTITUTION FOR MICROSYSTEMS AND SOLID STATE TECHNOLOGIES EMFT

FRAUNHOFER EMFT TECHNOLOGY OFFERING

Fraunhofer Research Institution for Microsystems and Solid State Technologies EMFT

Director: Prof. Dr. rer. nat. Christoph Kutter

Hansastraße 27 d
80686 München

contact@emft.fraunhofer.de
www.emft.fraunhofer.de

Contact:

Prof. Dr. Peter Kücher
Phone + 49 (0) 89 54759-241 | Fax -550
Peter.Kuecher@emft.fraunhofer.de

FRAUNHOFER EMFT TECHNOLOGY OFFERING

Fraunhofer EMFT has gathered a broad experience in the fields of silicon and foil technologies, extending several years back. Our offering includes:

- CMOS/MEMS-line (200 mm, structural resolution up to 0.35 µm)
- MEMS-line for non-CMOS compatible processes
- Assembly and interconnection technologies including heterogeneous system integration
- Processing on foil substrates

Additionally we can offer layout design and comprehensive process characterization. These technologies enable us to develop sensors, actuators, special components as well as circuits.

The services offering of Fraunhofer EMFT includes the following single processes as well as the resulting process sequences. In cooperation with our customers we also develop new processes respectively technologies on our equipment.

Additionally we are happy to provide technical consulting in the field of research and development, according to your needs.

Inhalt

Fraunhofer EMFT scientist working at a system for circuit design

1 Layout

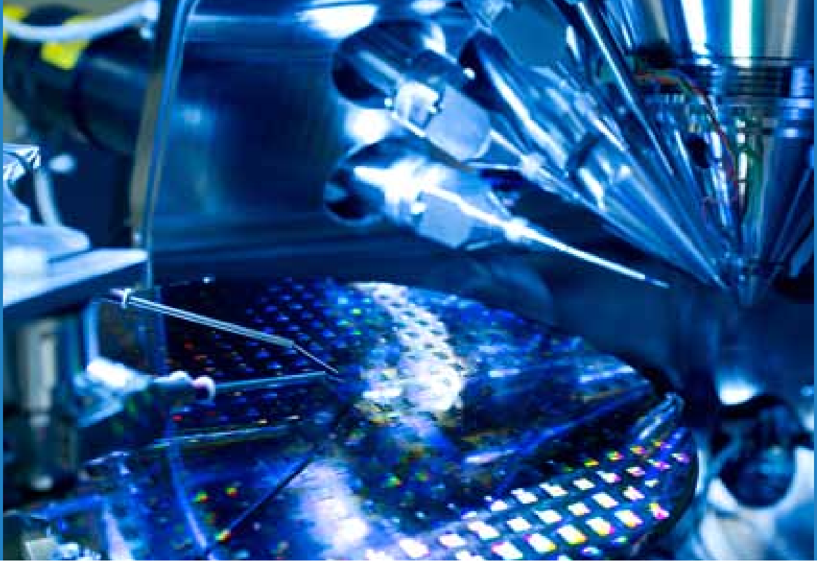
1.1 Mask layout

Special transistors, MEMS components, small circuit units etc., developed by Fraunhofer EMFT or by the customer, are implemented into a physical layout. This can then be directly used for mask creation by an external mask producer.

Layout tools of EDA solutions (Tanner EDA L-Edit) and Mentor Graphics (IC station) are used. Interfaces to mask shops for producing stepper reticles, masks for contact lithography and mask substrates for reel-to-reel foil technologies are established. Several layout formats are available for processing customized layouts, such as gds2, DXF, Gerber, drawn layout templates etc.

We have comprehensive experience with PCM (Process Control Monitor) structures.

Ready processed wafers (e.g. CMOS process of a foundry) can be processed further in order to implement the structures necessary for the Fraunhofer EMFT technologies on a complete layout. Examples hereof are the connection of Through-Silicon-Via (TSV) to the Re-Distribution Layer (RDL) for 3D integration or structures for on-top processes of preprocessed chips.



Fei Helios Nanolab for Focused Ion Beam

2 CMOS/MEMS-line

The contamination levels of all processes meet the CMOS standard.

2.1 Diffusion processes

2.1.1 Oxidation

Building up of SiO_2 layers, 4 nm to 3 µm thick, through wet or dry oxidation, optionally with HCl, in temperature range of 650 °C to 1250 °C. Wafer sizes of 150 mm and 200 mm can be processed. The processing takes place in horizontal oven Tempress TS8603. Tempress AtmoScan system is available for thin oxide layers.

2.1.2 Diffusion

Introduction of dopants, activating implantations, and spreading of BPSG layers in an inert or oxidizing atmosphere in temperature range of 650 °C to 1250 °C. Wafer sizes of 150 mm and 200 mm can be processed. The processing takes place in horizontal oven Tempress TS8603.

2.1.3 RTP (Rapid Thermal Processing)

Producing thin oxide layers, RNO layers, activating implantations, as well as silicidation. 200 mm wafers can be processed. The processing takes place in Mattson 2900RTP equipment.

2.2 Layer deposition

2.2.1 Poly- and amorphous silicon

LPCVD (Low Pressure Chemical Vapor Deposition) layer deposition of undoped polysilicon or amorphous silicon 50 nm to 3 µm thick in temperature range of 450 °C to 650 °C. Wafer sizes of 150 mm and 200 mm can be processed. The processing takes place in horizontal oven Tempress TS8603.

2.2.2 TEOS LPCVD-oxide

LPCVD (Low Pressure Chemical Vapor Deposition) layer deposition of silicon oxides 20 nm to 800 nm thick in temperature range of 450 °C to 650 °C. Wafer sizes of 150 mm and 200 mm can be processed. The processing takes place in horizontal oven Tempress TS8603.

2.2.3 LPCVD-nitride

LPCVD (Low Pressure Chemical Vapor Deposition) layer deposition of silicon nitride 20 nm to 250 nm thick in temperature range of 700 °C to 800 °C. Wafer sizes of 150 mm and 200 mm can be processed. The processing takes place in horizontal oven Tempress TS8603.

2.2.4 Doped poly-silicon

In-situ phosphor-doped poly-silicon 30 nm to 6 µm thick in temperature range of 400 °C to 800 °C. 200 mm wafers can be processed. The processing takes place in Altatech Alta-CVD.

2.2.5 Doped oxides

Deposition of BSG (Boron-Silicate Glass), PSG (Phosphor Silicate Glass) and BPSG (Boron-Phosphor Silicate Glass) for thickness of 50 nm to 2 µm in temperature range of 300 °C to 460 °C. 200 mm wafers can be processed. The processing takes place in Altatech Alta-CVD.

2.2.6 PECVD-oxide

PECVD (Plasma-Enhanced Chemical Vapor Deposition) of USG (Undoped Silicate Glass) for thickness of 30 nm to 3 µm in temperature range of 200 °C to 480 °C. 200 mm wafers can be processed. The processing takes place in AMAT P5000 CVD chambers (TEOS or SiH_4) or in Altatech Alta-CVD.

2.2.7 Ozon-TEOS SACVD

SACVD (Sub-Atmospheric Chemical Vapor Deposition) of silicon oxide layers 100 nm to 800 nm thick in temperature range of 300 °C to 480 °C. 200 mm wafers can be processed. The processing takes place in AMAT P5000 CVD chambers or in Altatech Alta-CVD.

2.2.8 PECVD-nitride

PECVD (Plasma Enhanced Chemical Vapor Deposition) of nitride layers 50 nm to 800 nm thick in temperature range of 300 °C to 400 °C. 200 mm wafers can be processed. The processing takes place in AMAT P5000 CVD chambers.

2.3 Metallization

2.3.1 Sputtering of AlSi, Ti, TiN

Deposition of AlSi, Ti and TiN in temperature range of 50 °C to 400 °C. The layer thickness can be customized according to individual needs. The layers can be combined at will. 200 mm wafers can be processed. The processing takes place in Oerlikon Clusterline 200.

2.3.2 MOCVD for TiN and CVD for tungsten

MOCVD (Metal-Organic Chemical Vapor Deposition) of highly compliant and insi-tu-compressed TiN layers 8 nm to 60 nm thick in temperature range of 340 °C to 430 °C. TDMAT is used as precursor.

CVD (Chemical Vapor Deposition) of highly compliant wolfram layers 100 nm to 800 nm thick in temperature range of 380 °C to 430 °C. WF_6 is used as precursor. Can be combined in-situ with TiN MOCVD, including back-etching of the tungsten and TiN layers (TSV-metallization).

200 mm wafers can be processed. The processing takes place in AMAT P5000 multi-chamber system.

2.4 Lithography

2.4.1 Spin-on / spray coating and development

i-Line-resist technology for coatings 700 nm to 10 µm thick. Before coating the wafers can be prepared with HMDS, in order to improve the adhesion of the coating on the substrate. 200 mm wafers can be processed. The processing takes place completely automatically in SÜSS Gamma.

2.4.2 i-Line lithography

Exposure of photo-sensitive layers at minimal lateral resolution of 0.35 µm. Maximum size of the exposure field 20 mm to 21 mm. 200 mm wafers can be processed. The exposure is done with i-Line-stepper Canon FPA 3000 i4.

2.4.3 Contact and proximity lithography

Exposure of i-Line-sensitive photoresist. The required 1:1 transfer of the structure of the shadow mask can be carried out using the requested distance (proximity) or with contact. Chrome masks are used. In addition to the standard incident light microscope, IR optics can be used for aligning the mask and the substrate. Wafer sizes of 150 mm and 200 mm can be processed. The processing takes place in the contact exposure device SÜSS MICROTEC MA8Gen3.

2.4.4 Double-sided exposure

Adjusted exposure of the back side of the substrate with adjustment accuracy in 2 µm range. Wafer sizes 150 mm and 200 mm can be processed. The processing takes place in the contact exposure device SÜSS MICROTEC MA8Gen3.

2.4.5 Electron beam lithography

Writing of structures smaller than 10 nm. Existing GDSII and CIF files can be read by the software and consequently utilized for structuring. After development the structure sizes can be specifically targeted and analyzed (REM capabilities). Wafer sizes of 100 mm, 150 mm and 200 mm can be processed. The processing takes place in Raith 150-TWO.

2.5 Dry-chemical etching

2.5.1 Reactive ion etching of dielectrics and polymers

Magnetically Enhanced Reactive Ion Etching (MERIE) processes for structuring or large-area etching of dielectric layers (silicon-dioxide, -nitride, PSG, BPSG) in a broad thickness range of 20 nm to 6 µm for structures smaller than 100 nm. Automatic end-point detection (open area more than 2 %). Wafer cooling using an electrostatic chuck. The etching rates for oxides lie in the range of 200 - 400 nm/min. Wafer sizes of 200 mm can be processed. The processing takes place in eMxP+ chambers from Applied Materials (AMAT Centura). Additionally a P5000 Mark 2 oxide etching chamber from Applied Materials (AMAT) is available.

2.5.2 Reactive ion etching for poly-silicon structuring

Inductively Coupled Reactive Ion Etching for structuring or large-area etching of doped or undoped amorphous or polycrystalline layers as well as silicides (e.g. transistor gate stacks) in the thickness range of 20 nm to 500 nm for structures smaller than 100 nm. 200 mm wafers can be processed. The processing takes place in a poly-DPS chamber from Applied Materials (AMAT Centura).

2.5.3 Reactive ion etching of conductive layers (AlSi, Ti, TiN, W)

TiN/AlSi/TiN/Ti structures up to 0.6 µm in width at metal thickness up to 1.5 µm (depending on the structure size) are possible. Additionally RIE-tungsten etching, structured and unstructured (W-Etchback). 200 mm wafers can be processed. The processing takes place in P5000 Mark 2 from Applied Materials (AMAT Centura) with an ASP chamber (Advanced Strip and Passivation).

2.5.4 High-rate silicon etching (Bosch process)

Deep Reactive Ion-Etching (DRIE) of bulk silicon with Bosch process for aspect ratios up to 20:1. Etching of MEMS structures with low aspect ratio at silicon etching rate of 10 µm/min to 20 µm/min (depending on the structure size). Etching of TSV (Through Silicon Vias) with aspect ratios up to 20:1 at a silicon etching rate of 2 µm/min to 5 µm/min (depending on the structure size). Additionally, silicon etching with single-step-process is available. Wafers sizes of 200 mm can be processed. The processing takes place in SPTS Pegasus.

2.6 Wet chemical processes

2.6.1 Wafer cleaning

Cleaning of wafers using bench processes and Spray Acid Tool infrastructure SAT 508 IT from Semitool. Effective removal of organic and non-organic contaminations (SC1, SC2, Caro's acid and HF-Dip). Residues of coating and polymers can be removed using acetone, isopropanol and EKC-265 in stainless steel basin with ultrasound. Wafer sizes of 150 mm and 200 mm can be processed.

2.6.2 Mechanical wafer cleaning

Mechanical removal of particles on wafers by brushing with various cleaning media. Wafer sizes of 200 mm can be processed. The processing takes place in Scrubber Ontrac DSS 200.

2.6.3 Isotropic etching processes

Structuring wet chemical etching with photoresist is possible for the following layers: poly-silicon, doped and undoped oxides as well as aluminium (Alu, AlSi and AlSiCu).

An unstructured wet chemical removal of the following layers is possible: poly-silicon, doped and undoped oxides, silicon-nitride, titan-nitride, titan, tungsten and aluminium as well as aluminium alloys.

Wafer sizes of 150 mm and 200 mm can be processed.

2.6.4 Spin-etching processes

Silicon etching and stress-relief etching using a mixture of nitric acid, phosphoric acid and hydrofluoric acid. Silicon oxide etching using hydrofluoric acid. Both processes can be used for the front as well as the backside of the wafer. Wafer sizes of 150 mm and 200 mm can be processed. The processing takes place in Spin Processor SEZ 203.

2.7 Ion implantation

Implantation of argon, hydrogen, arsenic, boron, fluor, BF_2 and phosphor in doses range from 1×10^{11} cm^2 to 1×10^{16} cm^2. The energy range is 5 keV to 250 keV for single charged ions. Additionally, implantation of up to three times charged ions with energies up to 750 keV is possible. Furthermore, the implantation angle of 0° to 45° as well as rotation of 0° to 360° can be realized. Wafer sizes of 100 mm, 150 mm and 200 mm can be processed. All implantations take place in VARIAN E500 medium current implanter.

2.8 Epitaxy

2.8.1 Epitaxy of Si and SiGe layers

Epitaxy of silicon and silicon-germanium layers in the RP-CVD Reactor (6 Torr to Atm). A low doping with boron and phosphor is possible, as well as deposition of highly intrinsic silicon (3000 Ohm cm). Wafer sizes of 200 mm can be processed. The processing takes place in ASM Epsilon 2000.

2.8.2 Low temperature epitaxy

Epitaxial deposition of silicon and silicon-germanium. The layer deposition and surface cleaning take place at temperatures of 450 °C and above. Wafer sizes of 200 mm can be processed. The processing takes place in equipment developed by the company Muegge especially for this purpose.

2.9 Chemical Mechanical Polishing (CMP)

Polishing of layers of oxide, silicon and polysilicon with IPEC AVANTI 472. Processing of copper with IPEC-Westech 372M. Wafer sizes of 150 mm and 200 mm can be processed.

2.10 Mechanical grinding

Grinding of silicon wafers or wafer stacks from 100 µm to maximum 2000 µm thick. Special carrier technologies make grinding of topographic wafers, processing of extreme thin MEMS wafer stacks, back-side grinding of cavities, or thinning of wafers down to 30 µm possible. Wafer sizes of 150 mm and 200 mm can be processed. The processing takes place in Disco DFG 850 and DFG 8540 equipment.

2.11 In-line process analysis

2.11.1 Atomic Force Microscope (AFM)

Measurement of surface roughness and step height of max. 5.5 µm. Samples up to the size of 200 mm can be measured. The measuring takes place in the Atomic Force Microscope (AFM) D(imension)5000 from Digital Instruments.

2.11.2 In-line REM and Focused Ion Beam

In-line REM (Schottky Emitter) and Focused Ion Beam (Ga-FIB) with EDX-analysis and Gas Injection System (GIS). Wafer sizes of 100 mm, 150 mm and 200 mm can be processed. The processing takes place in FEI Helios Nanolab 650.

2.11.3 Measurement of layer thickness

Ellipsometric thickness measurement of thin and transparent materials. Wafer sizes of 150 mm and 200 mm can be processed. The measurement takes place in KLA Tencor UV1280.

Spectrometric thickness measurement of silicon layers thinner than 100 µm and layers permeable for infrared light. Sample sizes of 150 mm and 200 mm can be processed. The processing takes place in OMT.

2.11.4 X-Ray Diffraction (XRD)

X-Ray Diffraction (XRD) including reflectometry, especially for measuring the silicon-germanium concentration and the relaxation. Wafer sizes of 200 mm can be processed. The processing takes place in Philips XPert PRO, model MRD XL.

2.11.5 Measurement of wafer thickness (contactless, capacitive)

Thickness measurement of silicon wafers or wafer stacks. The measurement range lies between 400 µm and 1400 µm. Additionally, the waferbow and layer stress can be determined. Wafer sizes of 150 mm and 200 mm can be processed. The measurement takes place in Eichhorn and Hausmann MX 203-8.

Wet chemical bench processing

3 MEMS line

Processing of non-CMOS-compatible wafers.

3.1 Diffusion processes

3.1.1 Oxidation

Building up of SiO_2 layers 40 nm up to 2 µm thick using wet and dry oxidation, optionally with trans-LC additive, in temperature range between 850 °C and 1100 °C. Wafer sizes of 100 mm and 150 mm can be processed. The processing takes place in Tempress Omega horizontal oven.

3.1.2 Diffusion

Activation of dopands and annealing of implantations in an inert or oxidizing atmosphere in temperature range between 650 °C and 1150 °C. Wafers sizes of 100 mm and 150 mm can be processed. The processing takes place in Tempress Omega horizontal oven.

3.1.3 Tempering

3.1.3.1
Forming gas tempering of metals in an atmosphere of nitrogen/hydrogen in temperature range between 380 °C and 450 °C. Tempering of metals in an inert or oxidizing atmosphere in temperature range between 380 °C and 650 °C. Wafer sizes of 100 mm and 150 mm can be processed. The processing takes place in Tempress Omega horizontal oven.

3.1.3.2
Tempering of wafer stacks after silicon fusion bonding at temperatures up to 1100 °C. Wafer sizes of 100 mm and 150 mm can be processed. The processing takes place in Tempress Omega horizontal oven.

3.1.3.3
Drying or tempering of substrates at temperatures up to 400 °C in air, vacuum or N_2-atmosphere. Wafer sizes of 100 mm, 150 mm and 200 mm can be processed. The processing takes place in plate-heated Heraeus oven.

3.2 Layer deposition

3.2.1 PECVD-oxide / nitride

PECVD (Plasma-Enhanced Chemical Vapor Deposition) of silane-based layers of silicon oxide and silicon nitride for thicknesses from 50 nm to 2 µm in temperature range between 100 °C und 320 °C. Wafer sizes of 100 mm (with a transfer wafer) and 150 mm can be processed. The processing takes place in chamber 1 of Unaxis Quadra D200R.

3.2.2 PECVD- a-Si / a-SiC

PECVD (Plasma-Enhanced Chemical Vapor Deposition) of amorphous silicon layers for thicknesses from 100 nm to 1500 nm at processing temperature of 320 °C. Stripping of silicon carbide layers 50 nm to 800 nm thick in temperature range of 100 °C to 320 °C. Wafer sizes of 100 mm (with a transfer wafer) and 150 mm can be processed. The processing takes place in chamber 2 of Unaxis Quadra D200R.

3.3 Metallization

3.3.1 Metal deposition by sputtering – equipment 1

Vertical sputtering equipment with two chambers, substrate conditioning by inverse sputter etching is possible in the lock. The coating chamber includes four targets for DC magnetron sputtering. Typical metals include Au, Al, Cr, Cu, Ni, Ti and TiW, additional metal targets are available or can be ordered and installed at request. The equipment allows for simultaneous coating of up to 12 wafers size 150 mm or smaller, or up to 8 wafers size 200 mm. Coating of foils or special components is also possible at request. The processing takes place in Balzers LLS801.

3.3.2 Metal deposition by sputtering – equipment 2

Metallization with common metals, metal oxides and alloys (Al, AlCu, Al_2O_3, SiO_2, Cr, NiCr, Ta, Pd, Ag, Ti, WTi and Cu) with specific requirement profiles. Additionally, layers of nitride or oxide can be produced using reactive sputtering processes. Optionally, the substrates can be actively heated during the process. A separate sputter etching chamber is available for etching. Wafers and flat samples up to the size of 200 mm can be processed. The processing takes place in the sputtering equipment CS850S from VON-ARDENNE.

3.3.3 Metal deposition by vapor deposition

Vapor deposition is done by thermic evaporization (1 source) or electron beam evaporization (2 sources with 4 material supplies each). Deposition of several different metals or metal oxides is possible, as well as preprocessing of the substrate surface by glow plasma. Quartz glass blasters enable heating of the layers before and during deposition. Static or rotation coating of the samples is possible. Wafers smaller than 150 mm in diameter can be processed (12 pieces), the carriers have to be adapted for other formats. The processing takes place in Balzers BAK 760.

3.3.4 Electroplating (Cu, Sn)

Electrolytic production of layers of pure copper and tin layers for contact metallization e.g. for wafer-to-wafer bonding processes. For the pattern plating processes photo resists 5 µm to 50 µm thick are structured on a thin Cu plating-base. Wafer sizes of 150 mm and 200 mm can be processed.

3.4 Lithography

3.4.1 Coating

Coating of the wafers with various coatings using a manually loadable spin-coater. Standard coatings include positive-working resists from Clariant (AZ1514H, AZ4500), for layers from 1.5 µm to 8 µm thick.

Wafers up to the size of 150 mm can be processed, special substrates upon request. The processing takes place in Convac spin-coater.

3.4.2 Drying

Drying of the coatings using Convac hotplate for wafers up to 150 mm and Heraeus convection oven for wafers up to 200 mm in size.

3.4.3 Exposure

Various exposure modi such as proximity, soft, hard and low-vacuum contact are possible. The backside-alignment system enables alignment of the mask to the alignment marks on the backside of the wafer. Teflon-coated chucks guarantee defect-free processing of double-sided polished wafers. Wafer sizes of 100 mm and 150 mm can be processed, special substrates upon request. The processing takes place in Süss mask-aligner MA5.

3.4.4 Special processes

Processing of dry-resists (DuPont, MX5015) (lamination in laboratory), double-layer lift-off process (under development).

3.5 Dry-etching

3.5.1 Reactive Ion Etching (RIE) of dielectrics

Reactive Ion Etching (RIE) processes for structuring of dielectric layers (silicon oxide, -nitride, - carbide) for thicknesses of 20 nm to 2 µm using CHF_3-, CF_4- and SF_6-based processes. The wafer cooling is carried out using He-backside cooling or mechanical wafer clamping on substrate holder. Wafer sizes of 150 mm can be processed. The processing takes place in RIE chamber of the STS cluster tool equipment.

3.5.2 High rate silicon etching (Bosch process)

Anisotropic deep etching of silicon, etching rate up to 3 µm/min ("Bosch process") and with aspect ratio up to 15:1 (D/W) using an ICP chamber (Inductively Coupled Reactive Ion Etching). Wafer sizes of 150 mm can be processed. The processing takes place in ICP chamber of STS cluster tool equipment.

3.5.3 Resist stripping

Stripping of resist layers using the ICT chamber (Inductively Coupled Reactive Ion Etching) of the STS cluster tool. Wafer sizes of 150 mm can be processed.

3.5.4 Reactive etching of dielectric and organic layers

Etching of various organic layers (coatings, dielectrics) and inorganic layers (Si, SiO, SiN, SiC) using a manual RIE system, connected to the process gases O_2, CF_4 and CHF_3 . Due to the manual loading, all substrates and formats up to 150 mm in diameter can be processed. The processing takes place in PlasmaLab from the Oxford Plasma company.

3.6 Wet chemical processes

3.6.1 Cleaning processes

SC1, SC2 and Caro cleaning as well as SiN etching processes (phosphoric acid) in heatable quartz basins.

HF Dip (1 %) and BOE etching of SiO_2 layers are carried out in basins. The standard for resist-stripping of positive resists is the AZ Remover 100 (supported by ultrasound).

3.6.2 Metal etching

Metal etching (for example Al, Cu, Cr, TiW, Au, Sn) is carried out in beakers. For processes in basins wafers up to 150 mm in size can be processed, in beakers also wafers the size of 200 mm can be processed.

3.6.3 KOH etching

KOH etching in tempered quartz glass vessels, filled with 10 liter etching material (33 % KOH). The etching temperature is 60 °C or 80 °C. Wafer sizes of 100 mm or 150 mm can be processed, as single wafers or in batches of 12.

3.7 In-line process analytics

3.7.1 Microscopy

Microscopy with incident light, dark field and interference contrast, image documentation via camera is possible. Wafer sizes of 100 mm, 150 mm, or 200 mm can be processed. A Leica microscope is used.

3.7.2 Reflectrometry

Reflectometry at wave lengths of 450 nm to 750 nm, minimum spot size approximately 20 µm. The reflectrometric measuring equipment is connected to the Leica microscope.

3.7.3 Profilometry

Measurement of steps from 50 nm to 300 µm. Samples up to 200 mm in diameter can be processed. The processing takes place with Veeco Dektak.

3.7.4 Measurement of wafer thickness and deflection

Measurement of wafer thickness and deflection using a contactless capacitive method. Samples up to 150 mm in diameter can be processed. The measurement takes place with equipment from the company Eichhorn&Hausmann.

3.7.5 Wetting angle

Measurement of the wetting angle by measuring the polar and dispersive components. The processing takes place in the laboratory with equipment from the company DataPhysics.

Fraunhofer EMFT scientist in the laboratory at the FCB3-Bonder

4 Assembly and interconnection technologies

4.1 Wafer bond

Silicon Fusion Bond (SFB) of wafers with Si or SiO_2 surfaces. Processing of the 100 mm or 150 mm wafers is carried out in the Süss BA6 bondaligner (alignment), Süss SB6 bondaligner (prebond) and in the Tempress oven (annealing). Processing of the 200 mm wafers takes place in the EV501 (prebond) and Tempress oven (annealing).

4.2 Single chip placement

Placement of chips on wafers and foil substrates. A thermocompression probe as well as an ultrasound probe are available for the equipment. Substrates up to 200 mm x 200 mm in size can be processed. The processing takes place in Panasonic FCB3.

4.3 Electroplating (Cu, Sn)

Electrolytic creation of pure copper and tin layers for contact metallization, e.g. for wafer-to-wafer bond processes. For the "pattern plating" processes photo resists from 5 µm to 50 µm thick are structured on thin Cu-PB –layers. Wafer sizes of 150 mm and 200 mm can be processed. Deposition of the copper layers takes place in Technotrans microfom.200, deposition of the tin layers in RENA EPM 201F.

4.4 Solid Liquid Interdiffusion (SLID)

Solid Liquid Interdiffusion of tin and copper for simultaneous assembly and electrical interconnection of two chips. This creates a high-melting intermetallic compound (Cu_3Sn, 450 °C), with a higher melting point than that of elementary tin (230 °C). This increase in the melting point through the SLID process enables a solid connection of both chips up to the new melting point.

4.5 Sawing

Separating of chips of defined index and size by sawing, also called dicing. Setting the optimum process parameters and selecting the saw blade depend on the thickness of the piece to be sawn as well as on the material of the sample. Samples up to 200 mm in diameter and 3 mm to 5 mm in thickness can be processed, depending on the saw blade used. The processing takes place in Disco wafer-saw 341.

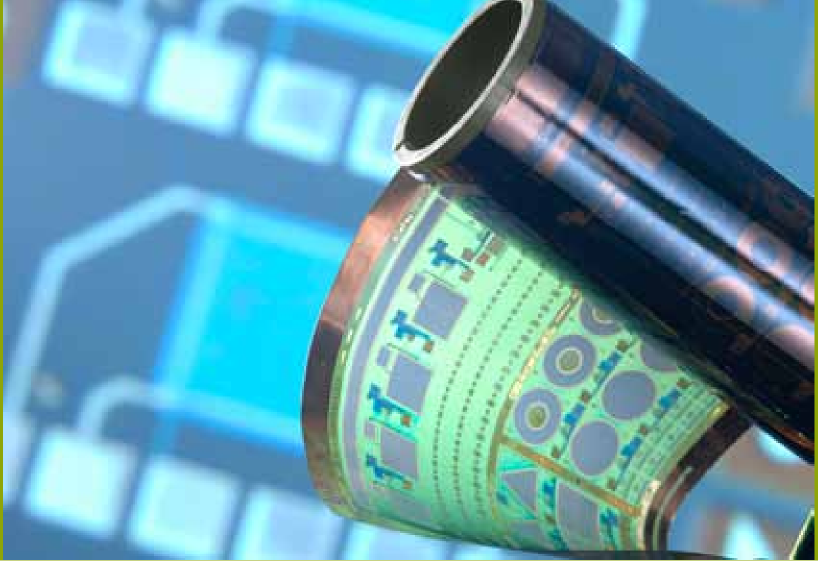
4.6 Wire bonding

4.6.1 Alu-wire bonding

Alu-wire bonding primarily for contacting gold-pads (circuit boards) or gold plugs on piezo electrodes (silver palladium). Wire material is AlSi (1 %) 25 µm thick in diameter. Bonding takes place at room temperature. The processing takes place in wire bonder from Kulicke & Soffa: 4523A Digital. A hand bonder is used for processing small batches.

4.6.2 Gold-wire bonding

Wire bonding for sequential contacting of semiconductor elements using the Thermosonic-Ball-Wedge method (TS-Bonding). For this method a 25 µm thick gold wire is used. The heating table can be heated up to 120 °C. The processing takes place in gold bonder from the company Kulicke and Soffa Europe GmbH. A hand bonder is used for processing small batches.



Prozessing of organic semiconductors using the reel-to-reel method

5 Microfabrication of foil substrates

The standard reel width is 215 mm, the size of the processing area is 200 x 200 mm^2.

5.1 Metallization

Metallization of foil substrates with adhesive and conductive layers, e.g. with copper or chrome, using a sputtering system. The coating is carried out reel-to-reel with maximum substrate width of 215 mm. The equipment from the company FHR additionally includes an IR heater for better outgassing of the layers, as well as inverse sputter etcher for surface activation.

5.2 Lamination

Lamination of various foils under pressure and temperature using heated reels. Typical applications are lamination of dry film resist for preparation of photolithographic structuring, or passivation with adhesive-coated covering foils. The adjustable process parameters include: temperature, pressure and feed rate. The processing takes place in equipment from the company Stork.

5.3 Coating

Coating using thin films, such as resist, dielectrics, and passivation from liquid phase on foil. In addition to coating chamber with a slot nozzle application unit, a drying line with infrared and convection heating is available. Homogenous layers thinner than 1 µm can be created as a continuous application process. Optical thickness measurement of thin layers is carried out using an ellipsometer and a reflectometer. The processing takes places in in-line coating equipment from the company Coatema.

5.4 Exposure

UV lithography for creating a mask structure in the resist of a layered foil system as a stop & go procedure. In addition to proximity and contact exposure the equipment includes an automatic pattern recognition for mask alignment. The equipment from the company Ciposa allows for processing or foil reels of 215 mm in width with 9” masks.

5.5 Development

For fixation and development of exposed resist layers a spray developer is used. At places, where no resist remains after the development, the metallization can be galvanically strengthened or etched. The processing takes place with equipment from the company Höllmüller.

5.6 Electroplating

Stripping of copper several µm thick on pre-metallized and structured polymer films (pattern plating), in a continuously operating galvanic equipment. The process is divided into pre-galvanic with low current and main galvanic with higher current.

5.7 Etching

Even etching of metallized foils in continuously operating spray-etch equipment. The modular construction enables fast change of etching medium, in order to be able to etch various metals. The processing takes place in equipment of the company Schmid.

5.8 Screen printing

Printing of various pastes (conductive paste, electroluminescence, dielectric, semiconductors) structured on a foil in a reel-to-reel screen printing equipment. In addition to subsequent drying with UV and convection, the equipment includes automatic pattern recognition capabilities for multilayer systems.

5.9 Laser processing

Processing of foils with a UV laser (355 nm). Local stripping of material from the covering layer as trenches or holes. Cutting through all foil layers is also possible. This enables opening vias, separating components from the composite foil, structuring layers, writing text or symbols for markings, or trimming film resistors. Alignment precision 50 µm. Processing is carried out with equipment from the company LS Systems.

5.10 Plasma etching

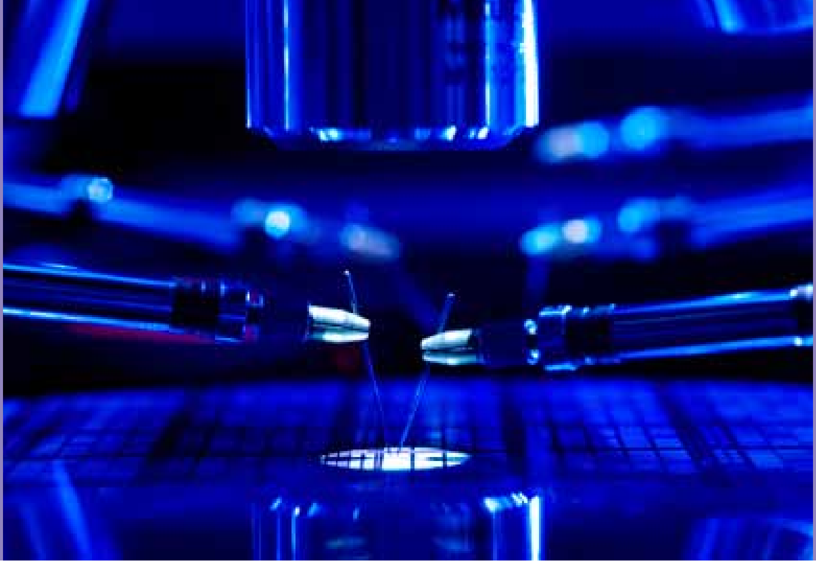
Surface conditioning and etching of foils and polymers. Coatings in reel-to-reel throughfeed process using plasma equipment. Nitrogen, oxygen and CF_4 are used as etching gases.

5.11 Rewinder

Winding of foil strips from one reel to the other, enabling exact merging and orthomorphic (true angles) cutting, parallel or perpendicular to the running direction of the foil. Left/right operation, web edge control, length measurement and adjustable strip tension enable optimal conditioning of the foil reels. The processing takes place with equipment from the company db-matic.

5.12 Pick & Laminate

Automatic assembly and electrical contacting of foil components (such as flexible batteries, displays, solar cells or other subsystems) on the base substrate, either on sheets or reels.



Wafer prober PA-200 for electrical characterization of PCM-structures

6 Process characterization

In addition to in-line process analytics, further process characterization methods are available at the Fraunhofer EMFT.

6.1 Sample preparation

6.1.1 Surface conditioning

As preparation for REM investigation, sample pieces of gold or gold/ palladium can be sputtered. Alternatively, carbon can be deposited. Samples up to approximately 70 mm in diameter can be processed. Plasma equipment for surface cleaning is available.

6.1.2 Target grinding

Target grinding of embedded preparations for sample preparation with grinding precision of 2 µm. Fragments up to 2 x 2 cm^2 in size can be processed. The processing takes place with StruersTargetSystem.

6.2 Electron beam analytics

6.2.1 Cambridge S-250

Scanning electron microscope (tungsten emitter) with EDX-accessory (Energy Dispersive X-ray spectroscopy). The detection is based on secondary electrons and backscattered electrons (BE).

6.2.2 Hitachi S4500

Scanning electron microscope (cold field emitter) with imaging resolution up to 1.5 nm. The detection is based on secondary electrons and backscattered electrons.

6.3 Wafer prober for electrical characterization of PCM structures

Electrical characterization of semiconductor components using an Agilent B1500A parameter analyzer system with up to five high resolution source- monitor units, a high resolution high power source-monitor unit, CV measurement capability (f up to 5 MHz) and two pulse generators, as well as a separate circuit matrix with up to twenty outputs for probecard applications. The wafer chuck can be heated up to 200 °C. 200 mm wafers can be processed. The characterization is carried out with a wafer prober measuring station PA-200, including darkbox, from the company Cascade Microtech.

Multi-layer bonds of a high-grade steel micro-pump

7 Manufacturing and testing technologies for microfluidic actuators

For developing and manufacturing of microfluidic actuators at the Fraunhofer EMFT two technology platforms are available:

- Silicon microfluidic actuators
- Stainless steel microfluidic actuators

The development platform for silicon utilizes the front-end process modules of the MEMS-line (see chapters above), whereas the development platform for stainless steel is currently being developed. Assembly of piezo-ceramic components on a silicon or stainless steel membrane is essential for both platforms.

7.1 Piezo assembly on wafer level

Assembly of piezo-ceramic elements on membranes (silicon or stainless steel) by gluing. A dispenser, controlled from an x-y-table, applies adhesive material at appropriate positions on the wafer. A pick & place module is used for placing the piezo-ceramic elements. Finally, the adhesive is cured.

7.2 Pre-tension of the piezo-ceramic elements

Specified pre-tension of the piezo-ceramic elements using a patented method. Due to the pre-tension the piezo-ceramic elements have an initial deflection after assembly. This method is important for manufacturing microfluidic actuators with extreme low dead volumes.

7.3 Fluidic test on wafer level

Fluidic characterization of pump chips on a complete assembled micropump wafer stack. The pump wafer is clamped in a device. An x-y-table is used for electrically contacting and controlling the upper side of the pump chips, whereas the fluidic contacts are created on the lower side. Characterization of the pump wafer with approximately 200 micropumps, including volume, production rate, counter pressure capability and leakage rate.

7.4 Silicon spraying

Spraying of thin silicone layers on substrates (silicon, stainless steel etc.) using an airbrush gun, controlled from an x-y-table. The silicone jet is shaded by shadow masks.

7.5 Topographic characterization of micromechanically produced structures

Characterization of micromechanical structures using an FRT topography measurement module, enabling 1D-, 2D- and 3D-measurements with measurement resolution up to 50 nm. The measurement module is controlled from an x-y-table. In addition to static measurements also dynamic measurements up to 15 kHz are possible.

7.6 Fluidic characterization of microfluidic components

Gravimetric measurement of production rate (several scales with various resolutions down to 0.1 µg are available). Various anemometric flow sensors for liquids and gases, automatic counter pressure measurement. Experience with various materials (water, air, oil, solvents and others). Measurement of minimum leakage rates (optically or capacitively) down to the µl/h range.